

Module timetable - Circuit Design Analysis & Testing (Wk 21, wk starting 23/12/2024)

		08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
We	25/12/2024	University cl Unavailable	losed e, Wk 21	'	'	'	'	'	'	'	'	'	'	
>	- 1													
hu	2/2024	University cludes Unavailable	losed e, Wk 21											
—	26/1													
Fri	27/12/2024	University c	losed e, Wk 21		'	'	'	'	'	'	'	'	'	
	27/1													
Sat	28/12/2024	University cludes Unavailable												
S														
Sun	2/2024	University cl Unavailable	losed e, Wk 21	,	,		,	,	,	,		,	,	
S	29/1													



Module timetable - Circuit Design Analysis & Testing (Wk 22, wk starting 30/12/2024)

		08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM		
Mo	2/2024	University of Unavailable	losed e, Wk 22	'	'	'	'	'	'	,		<u>'</u>		'		
2	30/1															
ne	2/2024	University closed Unavailable, Wk 22														
—	31/1															
We	1/01/2025	University of Unavailable	niversity closed navailable, Wk 22													
>	01/0															



Module timetable - Circuit Design Analysis & Testing (Wk 26, wk starting 27/01/2025)

		08:00AM	09:00A	И 10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
U R				Lecture, 09:30AM-12:00PM, Wk 26 Module: ENG790 (Circuit										
Th	30/01/2		D	lodule: ENG790 esign Analysis & taff: Sharp, And	& Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 27, wk starting 03/02/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 06/02/2025		Wk : Modu Design	ure, 09:30AM 27 ule: ENG790 gn Analysis & : Sharp, And	(Circuit & Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 28, wk starting 10/02/2025)

	08:00AM	09:00AM	1 10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 13/02/2025		W Mo De	ecture, 09:30AM k 28 odule: ENG790 esign Analysis & aff: Sharp, And	(Circuit & Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 29, wk starting 17/02/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
u 2025			Lecture, 09:30AM-12:00PM, Wk 29 Module: ENG790 (Circuit										
Th 20/02/2		Desi	ule: ENG790 gn Analysis 8 f: Sharp, Andi	k`Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 30, wk starting 24/02/2025)

		08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu	(02/2025		Wk Mod	ure, 09:30AM 30 ule: ENG790 gn Analysis 8	(Circuit									
	27,			: Sharp, And										



Module timetable - Circuit Design Analysis & Testing (Wk 31, wk starting 03/03/2025)

	08:	:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
	070			Lecture, 09:30AM-12:00PM, Wk 31 Module: ENG790 (Circuit										
⊢ }	06/03/2		Des Staf	lule: ENG790 ign Analysis & f: Sharp, Andr m: <u>E2</u>	(Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 32, wk starting 10/03/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
J 025			Lecture, 09:30AM-12:00PM, Wk 32 Module: ENG790 (Circuit										
Thu 13/03/2		Desi Staff	ule: ENG790 gn Analysis 8 : Sharp, Andı m: <u>E2</u>	(Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 33, wk starting 17/03/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
1025			Lecture, 09:30AM-12:00PM, Wk 33 Module: ENG790 (Circuit										
Thu		Desig	gn Analysis <mark>8</mark> : Sharp, Andı	(Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 34, wk starting 24/03/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 27/03/2025		Wk : Modu Desig	ure, 09:30AM 34 ule: ENG790 gn Analysis & : Sharp, And	(Circuit & Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 35, wk starting 31/03/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 03/04/2025		Wk : Modu Desig	ure, 09:30AM 35 ule: ENG790 gn Analysis & : Sharp, And	(Circuit & Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 36, wk starting 07/04/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
J 025		Lecti Wk	ure, 09:30AM 36	-12:00PM,									
Thu 10/04/2		Desi Staff	ule: ENG790 gn Analysis 8 : Sharp, Andı m: <u>E2</u>	(Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 37, wk starting 14/04/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
- ri 4/2025	Bank Holida Unavailable												
F													



Module timetable - Circuit Design Analysis & Testing (Wk 38, wk starting 21/04/2025)

		08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Mo	4/2025	Bank Holiday Unavailable, Wk 38												
2	21/0													
ne	4/2025	University c Unavailable	losed e, Wk 38											
\vdash	22/04/													



Module timetable - Circuit Design Analysis & Testing (Wk 39, wk starting 28/04/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
7		Lecti Wk	ure, 09:30AM 39	-12:00PM,									
Thu	\	Desi Staff	ule: ENG790 gn Analysis & f: Sharp, Andı m: <u>E2</u>	(Testing)									



Module timetable - Circuit Design Analysis & Testing (Wk 40, wk starting 05/05/2025)

		08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
40	5/2025	Bank Holida Unavailable	ank Holiday navailable, Wk 40											
2	02/0													
Thu	08/05/2025		Wk 4 Modu Analy	te Exam, 09:340 ule: ENG790 ysis & Testing Sharp, Andr	(Circuit Desi									



Module timetable - Circuit Design Analysis & Testing (Wk 43, wk starting 26/05/2025)

4o		08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
	5/2025	Bank Holida Unavailable												
2	26/0													



Module timetable - Circuit Design Analysis & Testing (Wk 4, wk starting 25/08/2025)

4o		08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
	8/2025	Bank Holida Unavailable												
_	25/0													