TT_2425_live

Module timetable - Circuit Design Analysis & Testing (Wk 21, wk starting 23/12/2024)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
We 25/12/2024	University closed Unavailable, Wk 21												
Thu 26/12/2024	University closed Unavailable, Wk 21												
Fri 27/12/2024	University closed Unavailable, Wk 21												
Sat 28/12/2024	University closed Unavailable, Wk 21												
Sun 29/12/2024	University closed Unavailable, Wk 21												

CELCAT web publisher

Module timetable - Circuit Design Analysis & Testing (Wk 22, wk starting 30/12/2024)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Mo 30/12/2024	University closed Unavailable, Wk 22												
Tue 31/12/2024	University closed Unavailable, Wk 22												
We 01/01/2025	University closed Unavailable, Wk 22												

CELCAT web publisher

Module timetable - Circuit Design Analysis & Testing (Wk 26, wk starting 27/01/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 30/01/2025		Lecture, 09:30AM-12:00PM, Wk 26 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew											

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Module timetable - Circuit Design Analysis & Testing (Wk 27, wk starting 03/02/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 06/02/2025		Lecture, 09:30AM-12:00PM, Wk 27 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew											

CELCAT web publisher

Module timetable - Circuit Design Analysis & Testing (Wk 28, wk starting 10/02/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 13/02/2025		Lecture, 09:30AM-12:00PM, Wk 28 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew											

CELCAT web publisher

Module timetable - Circuit Design Analysis & Testing (Wk 29, wk starting 17/02/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 20/02/2025		Lecture, 09:30AM-12:00PM, Wk 29 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew											

CELCAT web publisher

Module timetable - Circuit Design Analysis & Testing (Wk 30, wk starting 24/02/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 27/02/2025		Lecture, 09:30AM-12:00PM, Wk 30 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew											

CELCAT web publisher

Module timetable - Circuit Design Analysis & Testing (Wk 31, wk starting 03/03/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 06/03/2025		Lecture, 09:30AM-12:00PM, Wk 31 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew Room: E2											

CELCAT web publisher

Module timetable - Circuit Design Analysis & Testing (Wk 32, wk starting 10/03/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 13/03/2025		Lecture, 09:30AM-12:00PM, Wk 32 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew Room: E2											

Module timetable - Circuit Design Analysis & Testing (Wk 33, wk starting 17/03/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 20/03/2025		Lecture, 09:30AM-12:00PM, Wk 33 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew Room: E2											

CELCAT web publisher

Module timetable - Circuit Design Analysis & Testing (Wk 34, wk starting 24/03/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 27/03/2025		Lecture, 09:30AM-12:00PM, Wk 34 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew											

Module timetable - Circuit Design Analysis & Testing (Wk 35, wk starting 31/03/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 03/04/2025		Lecture, 09:30AM-12:00PM, Wk 35 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew											

Module timetable - Circuit Design Analysis & Testing (Wk 36, wk starting 07/04/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 10/04/2025		Lecture, 09:30AM-12:00PM, Wk 36 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew Room: E2											

Module timetable - Circuit Design Analysis & Testing (Wk 37, wk starting 14/04/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Fri 18/04/2025	Bank Holiday Unavailable, Wk 37												

Module timetable - Circuit Design Analysis & Testing (Wk 38, wk starting 21/04/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Mo 21/04/2025	Bank Holiday Unavailable, Wk 38												
Tue 22/04/2025	University closed Unavailable, Wk 38												

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Module timetable - Circuit Design Analysis & Testing (Wk 39, wk starting 28/04/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Thu 01/05/2025		Lecture, 09:30AM-12:00PM, Wk 39 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew Room: E2											

Module timetable - Circuit Design Analysis & Testing (Wk 40, wk starting 05/05/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Mo 05/05/2025	Bank Holiday Unavailable, Wk 40												
Thu 08/05/2025		Online Exam, 09:30AM-12:30PM, Wk 40 Module: ENG790 (Circuit Design Analysis & Testing) Staff: Sharp, Andrew											

Module timetable - Circuit Design Analysis & Testing (Wk 43, wk starting 26/05/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Mo 26/05/2025	Bank Holiday Unavailable, Wk 43												

Module timetable - Circuit Design Analysis & Testing (Wk 4, wk starting 25/08/2025)

	08:00AM	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM	05:00PM	06:00PM	07:00PM	08:00PM
Mo 25/08/2025	Bank Holiday Unavailable, Wk 4												